

G41T-M

Ver. 7.1

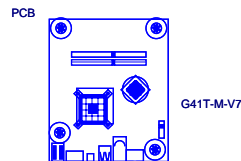
History :

06/26 -> Version A release.

08/11 -> 1.0 Release
P09. Modify ER38 from 24.9 ohm to 30.1ohm for SATA signal.
P27. Modufy ER68, ER69, ER73, C153 to larger value for fix S3 wake up in-rush current issue.
P29. Fixschematic ISP, ISN error issue.
P29. Modify damping resistor to 2.2 ohm and del VIN MLCC.

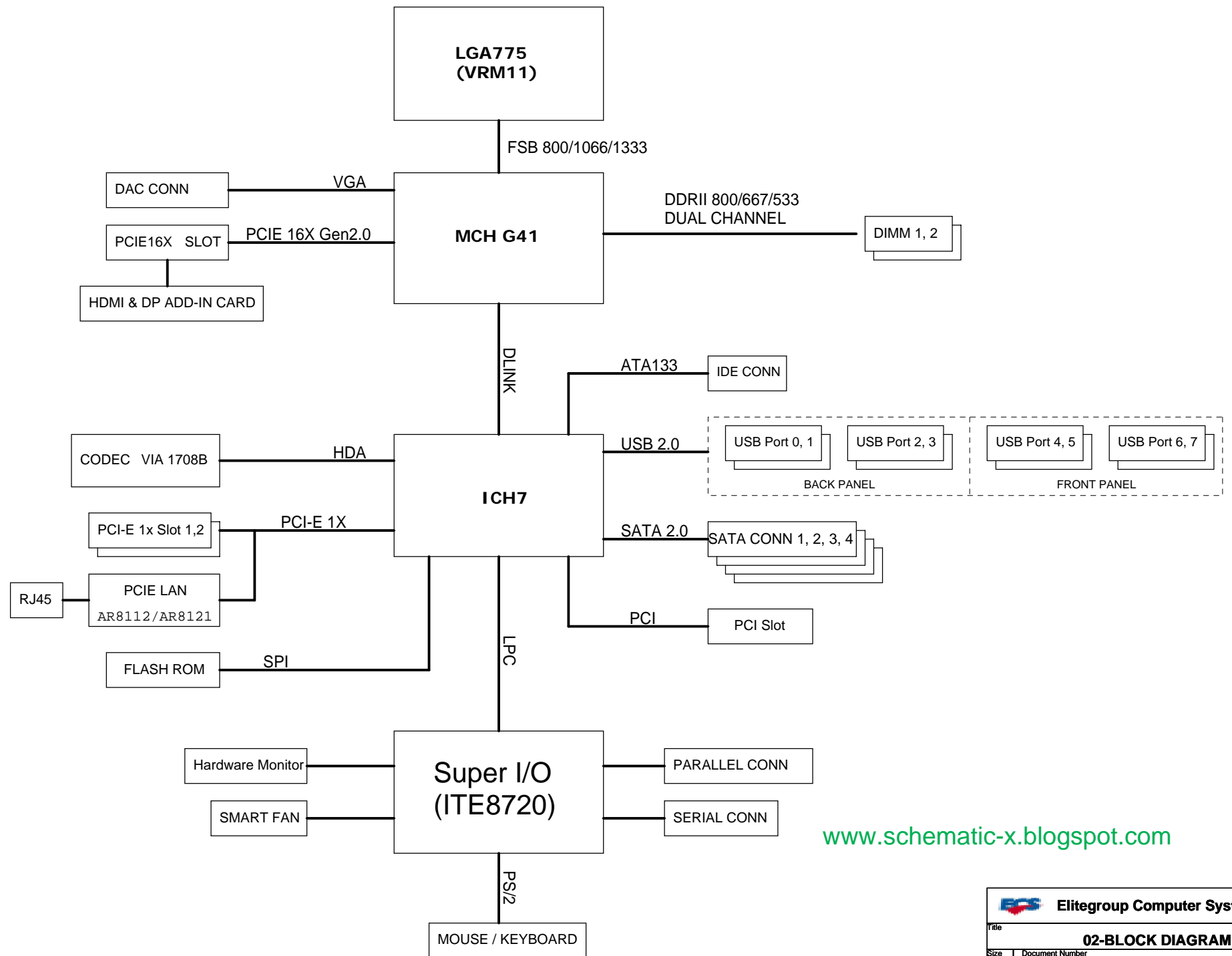
09/08 -> 1.0A Release
P23. Remove RN43,44,45 LPT damping resisters
P23. Connectot SB THERM- to SIO GPIO to tupport Shutdown Temperature
P30. Connectting ATX_PWRGD to P23 SIO.95pin

10/02 -> 1.9 Release
P29. Modify VCORE MOS to up1-down2 to support 95W CPU

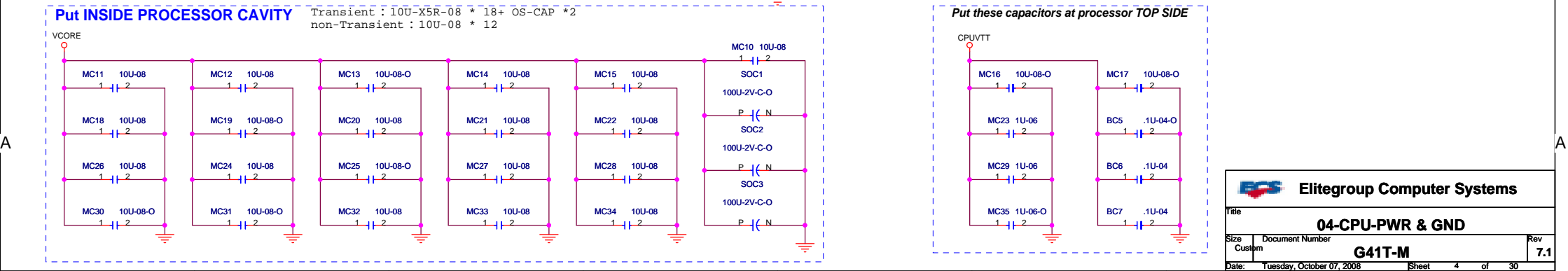
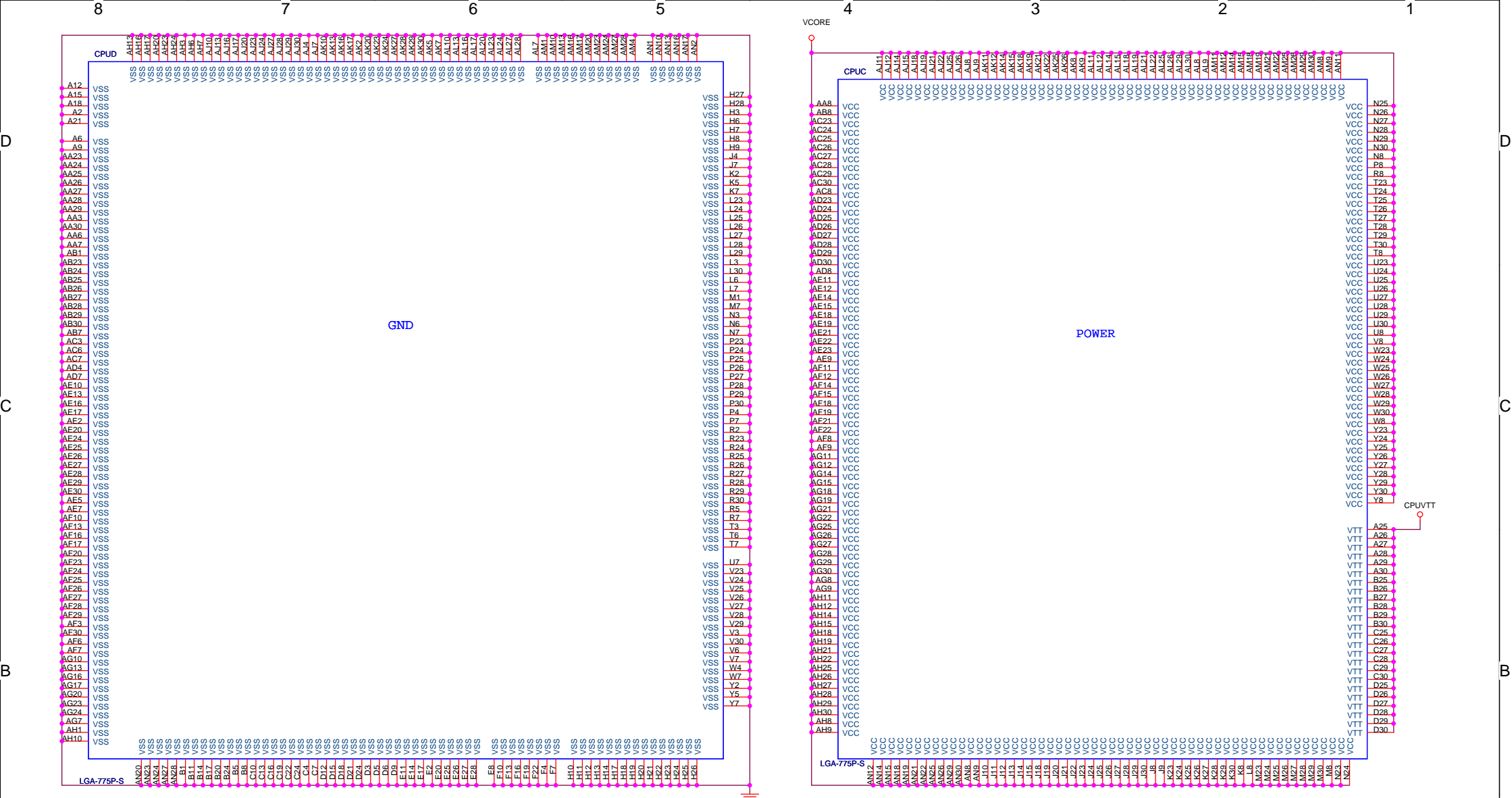


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HOST

3	HDSTBP-[0..3]	>>	HDSTBP-[0..3]
3	HD-[0..63]	>>	HD-[0..63]
3	HA-[3..35]	>>	HA-[3..35]
3	HDSTBN-[0..3]	>>	HDSTBN-[0..3]
3	HREQ-[0..4]	>>	HREQ-[0..4]
3	HDBI-[0..3]	>>	HDBI-[0..3]
3	HRS-[0..2]	>>	HRS-[0..2]
3	HADSTB-[0..1]	>>	HADSTB-[0..1]
3	HADS-	>>	HADS-
3	HTRDY-	>>	HTRDY-
3	HDRDY-	>>	HDRDY-
3	HDEFER-	>>	HDEFER-
3	HITM-	>>	HITM-
3	HIT-	>>	HIT-
3	HLOCK-	>>	HLOCK-
3	HBREQ0-	>>	HBREQ0-
3	HBNR-	>>	HBNR-
3	HBPRI-	>>	HBPRI-
3	HDBSY-	>>	HDBSY-
3	CPURST-	>>	CPURST-

12	HCLK_NB_P	>>	HCLK_NB_P
12	HCLK_NB_N	>>	HCLK_NB_N

HA-3	L36	FSB_AB_3
HA-4	L37	FSB_AB_4
HA-5	J38	FSB_AB_5
HA-6	F40	FSB_AB_6
HA-7	H39	FSB_AB_7
HA-8	L38	FSB_AB_8
HA-9	L43	FSB_AB_9
HA-10	N35	FSB_AB_10
HA-11	N37	FSB_AB_11
HA-12	J41	FSB_AB_12
HA-13	N40	FSB_AB_13
HA-14	M45	FSB_AB_14
HA-15	R34	FSB_AB_15
HA-16	R36	FSB_AB_16
HA-17	R37	FSB_AB_17
HA-18	R38	FSB_AB_18
HA-19	R39	FSB_AB_19
HA-20	R40	FSB_AB_20
HA-21	R41	FSB_AB_21
HA-22	R42	FSB_AB_22
HA-23	R43	FSB_AB_23
HA-24	R44	FSB_AB_24
HA-25	R45	FSB_AB_25
HA-26	R46	FSB_AB_26
HA-27	R47	FSB_AB_27
HA-28	R48	FSB_AB_28
HA-29	R49	FSB_AB_29
HA-30	R50	FSB_AB_30
HA-31	R51	FSB_AB_31
HA-32	R52	FSB_AB_32
HA-33	R53	FSB_AB_33
HA-34	R54	FSB_AB_34
HA-35	R55	FSB_AB_35

HREQ-0	G38	FSB_REQB_0
HREQ-1	K35	FSB_REQB_1
HREQ-2	J39	FSB_REQB_2
HREQ-3	C43	FSB_REQB_3
HREQ-4	G39	FSB_REQB_4

HADSTB-0	J40	FSB_ADSTBB_0
HADSTB-1	T39	FSB_ADSTBB_1

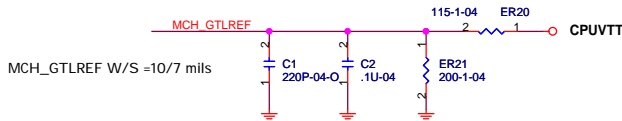
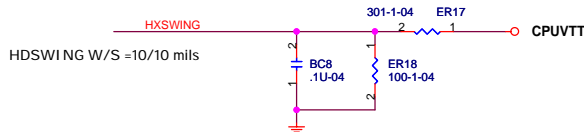
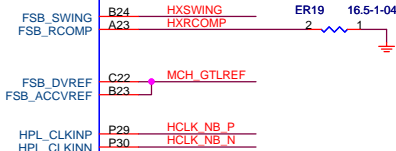
HDSTBP-0	C39	FSB_DSTBPR_0
HDSTBN-0	B39	FSB_DSTBNB_0
HDBI-0	B40	FSB_DINVB_0
HDSTBP-1	K31	FSB_DSTBPR_1
HDSTBN-1	J31	FSB_DSTBNB_1
HDBI-1	F33	FSB_DINVB_1
HDSTBP-2	J25	FSB_DSTBPR_2
HDSTBN-2	K25	FSB_DSTBNB_2
HDBI-2	F26	FSB_DINVB_2
HDSTBP-3	C32	FSB_DSTBPR_3
HDSTBN-3	D32	FSB_DSTBNB_3
HDBI-3	D30	FSB_DINVB_3

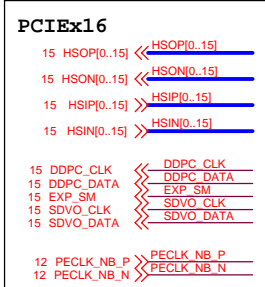
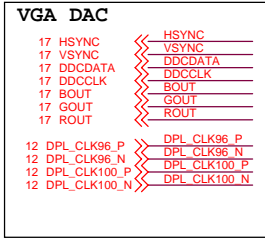
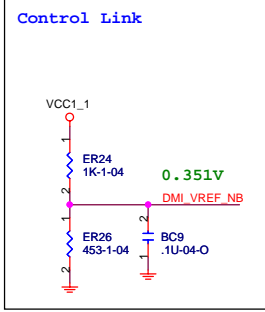
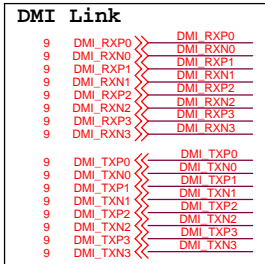
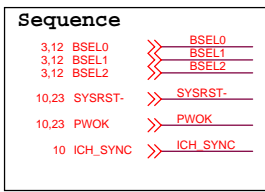
HADS-	J42	FSB_ADSB
HTRDY-	L40	FSB_TRDYB
HDRDY-	J43	FSB_DRDYB
HDEFER-	G44	FSB_DEFERB
HITM-	K44	FSB_HITMB
HIT-	H45	FSB_HITB
HLOCK-	H40	FSB_LOCKB
HBREQ0-	L42	FSB_BREQ0B
HBNR-	J44	FSB_BNRB
HBPRI-	H37	FSB_BPRIB
HDBSY-	H42	FSB_DBSYB
HRS-0	G43	FSB_RSB_0
HRS-1	L44	FSB_RSB_1
HRS-2	G42	FSB_RSB_2
CPURST-	D27	FSB_CPURSTB

STP_NB_N1	N25	RSVD_05
TP	C1	1 OF 9

AC82G41-A3

FSB_DB_0	F44	HD-0
FSB_DB_1	C44	HD-1
FSB_DB_2	D44	HD-2
FSB_DB_3	C41	HD-3
FSB_DB_4	E43	HD-4
FSB_DB_5	B43	HD-5
FSB_DB_6	D40	HD-6
FSB_DB_7	B42	HD-7
FSB_DB_8	B38	HD-8
FSB_DB_9	E38	HD-9
FSB_DB_10	A38	HD-10
FSB_DB_11	B37	HD-11
FSB_DB_12	D38	HD-12
FSB_DB_13	C37	HD-13
FSB_DB_14	D37	HD-14
FSB_DB_15	B36	HD-15
FSB_DB_16	E37	HD-16
FSB_DB_17	J35	HD-17
FSB_DB_18	H35	HD-18
FSB_DB_19	E37	HD-19
FSB_DB_20	G37	HD-20
FSB_DB_21	J33	HD-21
FSB_DB_22	L33	HD-22
FSB_DB_23	G33	HD-23
FSB_DB_24	L31	HD-24
FSB_DB_25	M31	HD-25
FSB_DB_26	M30	HD-26
FSB_DB_27	J30	HD-27
FSB_DB_28	G31	HD-28
FSB_DB_29	K30	HD-29
FSB_DB_30	M29	HD-30
FSB_DB_31	G30	HD-31
FSB_DB_32	J29	HD-32
FSB_DB_33	F29	HD-33
FSB_DB_34	H29	HD-34
FSB_DB_35	L25	HD-35
FSB_DB_36	K26	HD-36
FSB_DB_37	L29	HD-37
FSB_DB_38	J26	HD-38
FSB_DB_39	M26	HD-39
FSB_DB_40	H26	HD-40
FSB_DB_41	F25	HD-41
FSB_DB_42	G24	HD-42
FSB_DB_43	G25	HD-43
FSB_DB_44	H24	HD-44
FSB_DB_45	L24	HD-45
FSB_DB_46	J24	HD-46
FSB_DB_47	N24	HD-47
FSB_DB_48	C28	HD-48
FSB_DB_49	B31	HD-49
FSB_DB_50	F35	HD-50
FSB_DB_51	C35	HD-51
FSB_DB_52	B35	HD-52
FSB_DB_53	D35	HD-53
FSB_DB_54	D31	HD-54
FSB_DB_55	A34	HD-55
FSB_DB_56	B32	HD-56
FSB_DB_57	F31	HD-57
FSB_DB_58	D28	HD-58
FSB_DB_59	A29	HD-59
FSB_DB_60	C30	HD-60
FSB_DB_61	B30	HD-61
FSB_DB_62	E27	HD-62
FSB_DB_63	B28	HD-63





For G41 Only :

CL_CLK and CL_DATA No Connect

CL_RST# Connect to PLTRST#

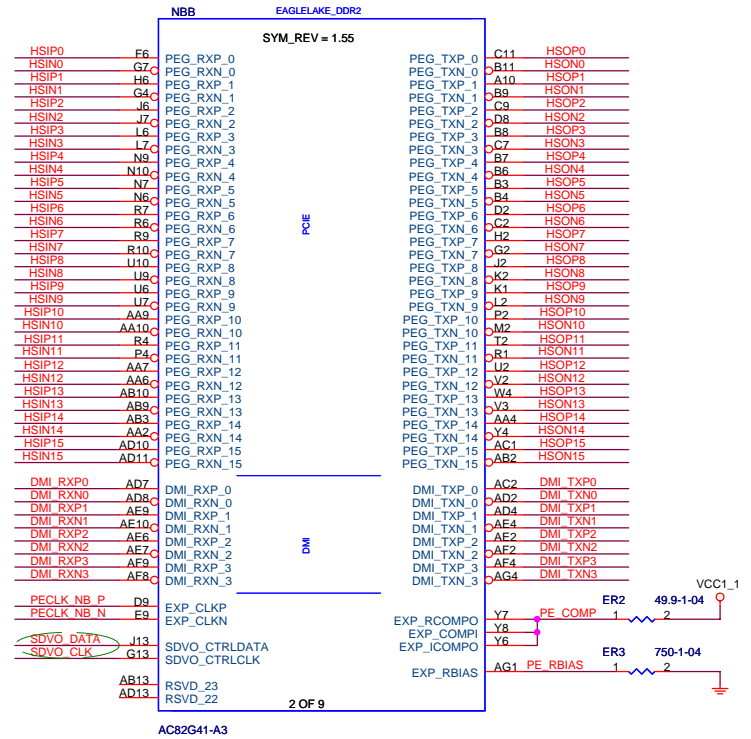
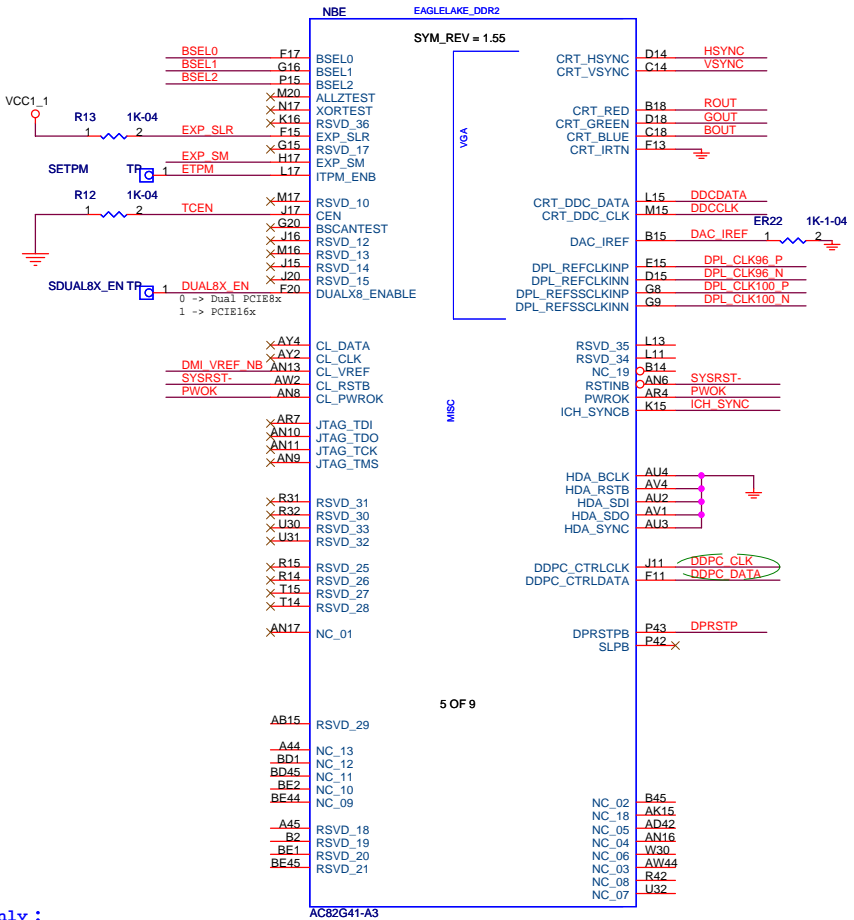
CL_VREF achieve 0.352 reference voltage

CL_PWROK Connect to PWOK

VCC_CL Connect to 1.1V GMCH core voltage

TPM1.2 STRAPS TABLE			
	ENABLE	DISABLE	DESCRIPTION
ETPM	L	Floating	TPM1.2 on MCH In MCH Pin.L17
SPIDO	H	Floating	TPM1.2 on ICH10 In ICH10 Pin.C26
TPM_PP	H	L	TPM Physical Presence In ICH Pin.C12

GMCH STRAPS TABLE			
	H	L	DESCRIPTION
EXP_SLR	NORMAL/ ATX	REVERSE/ BTX	PCI EXPRESS STATIC LANE REVERSAL
EXP_SM	CONCURRENT	NON-CONCURRENT	PCI EXPRESS / SDVO COEXISTENCE
TCEN	ENABLE	DISABLE	TLS CONFIDENTIALITY



Strapping

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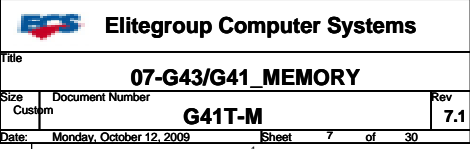
06-G43/G41_DMI/PCIe/DAC/HDMI

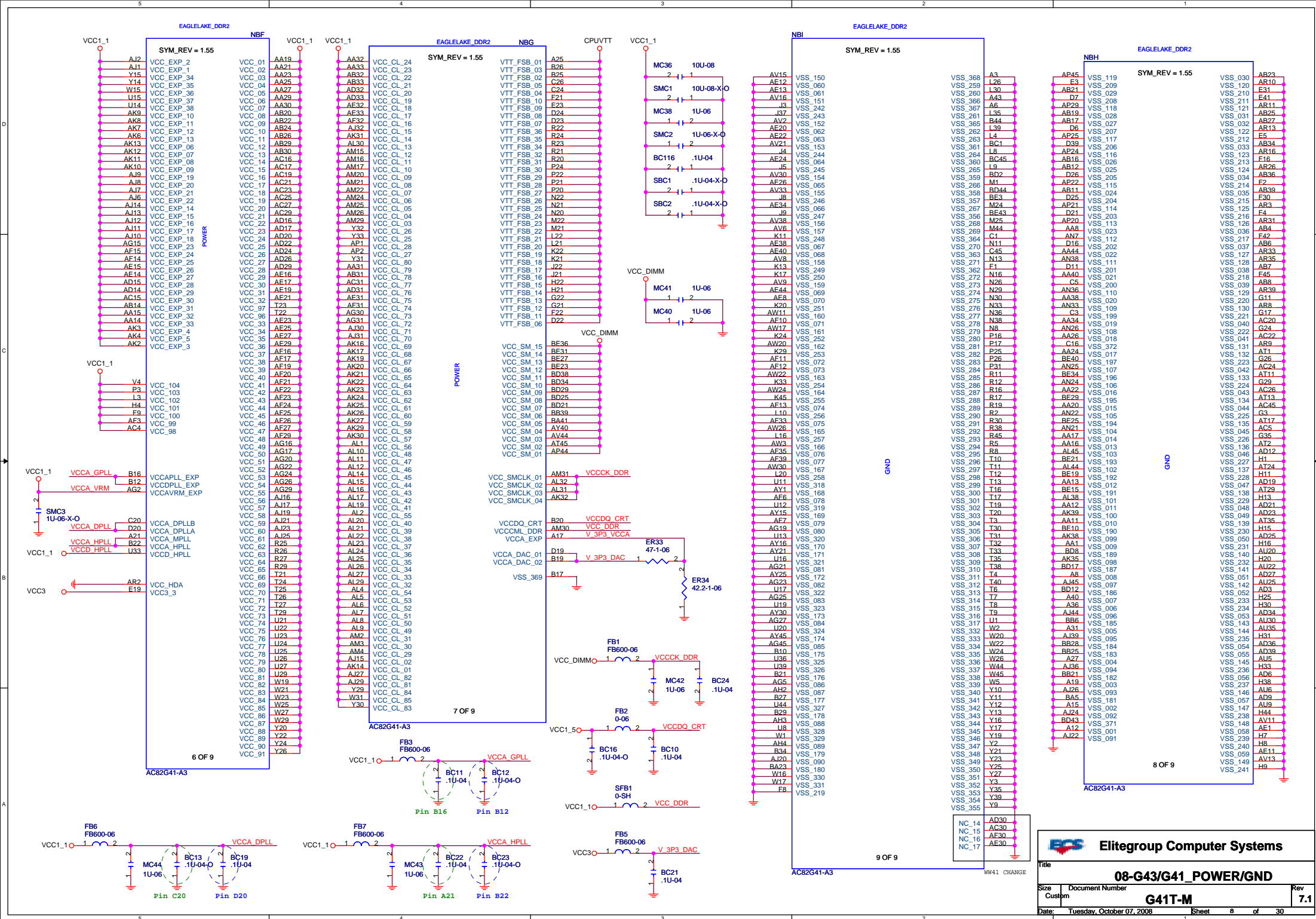
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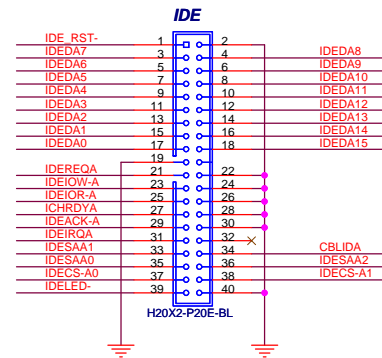
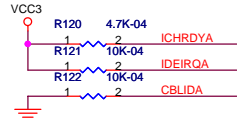
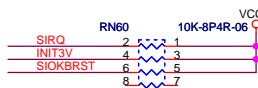
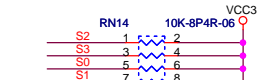
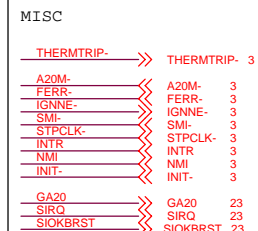
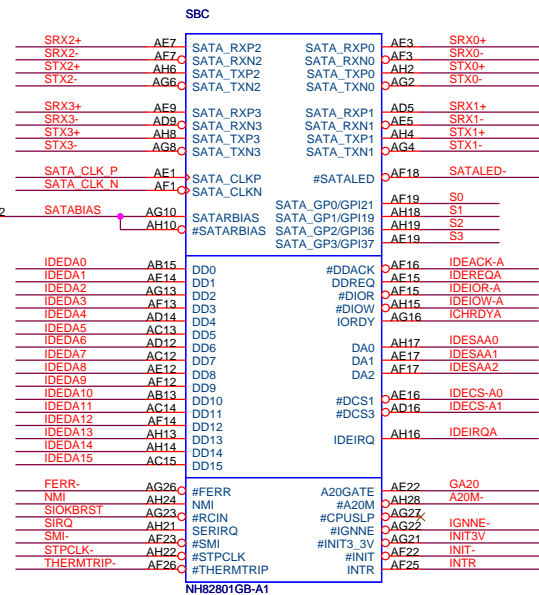
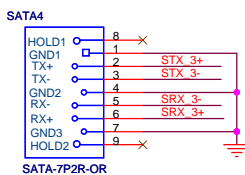
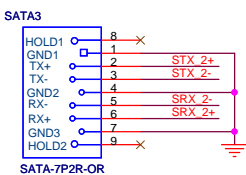
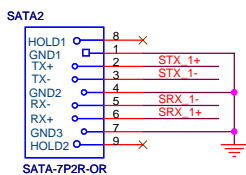
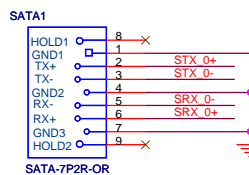
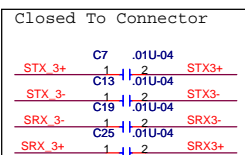
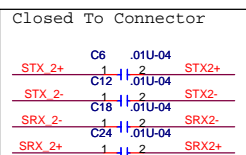
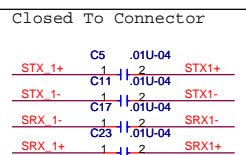
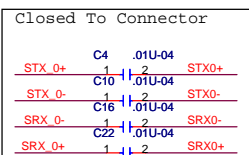
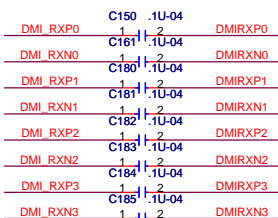
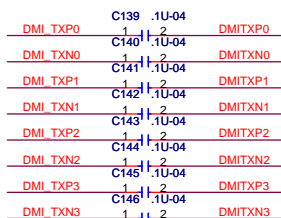
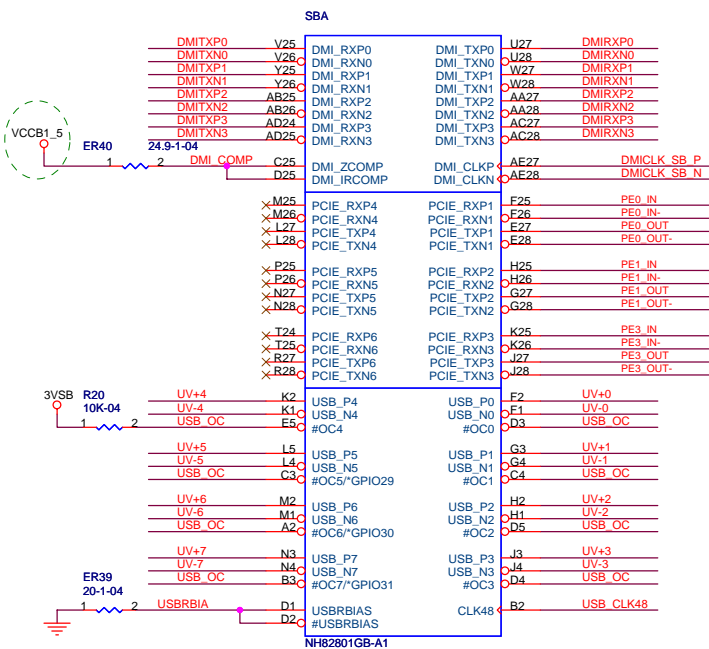
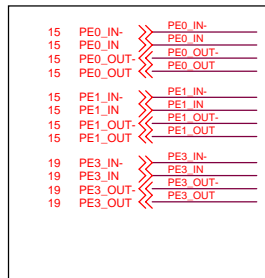
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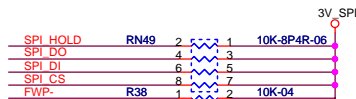
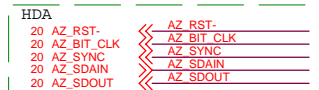
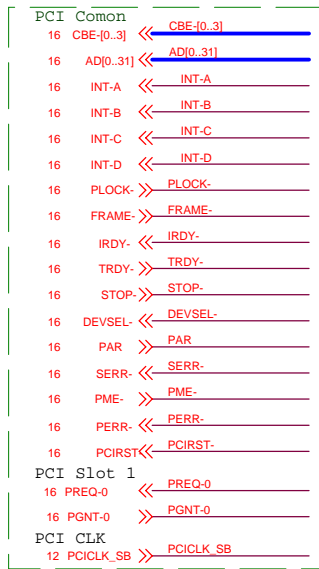
Monday, October 12, 2009

Sheet 6 of 30

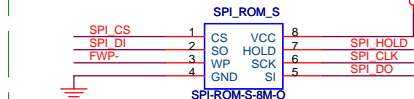
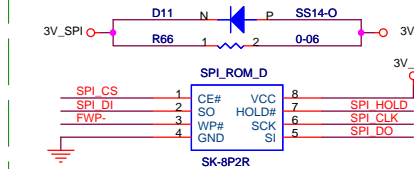






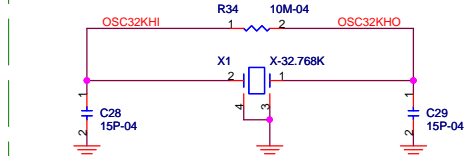


SPI ROM

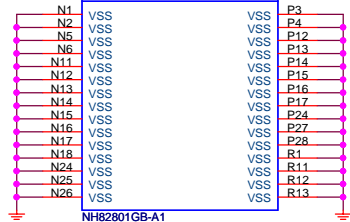
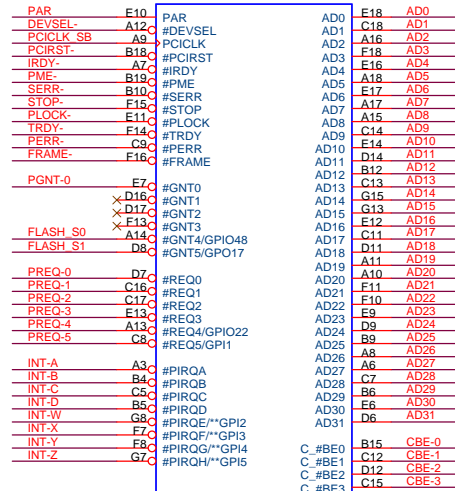


RTC CLK

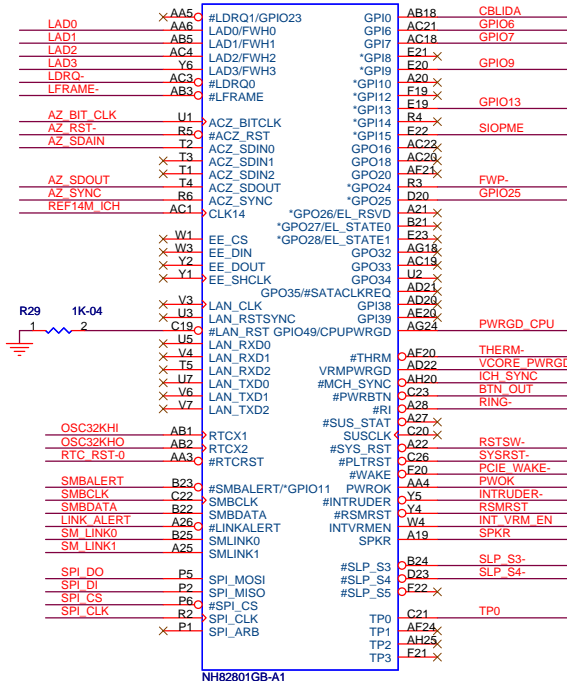
closed to chipset



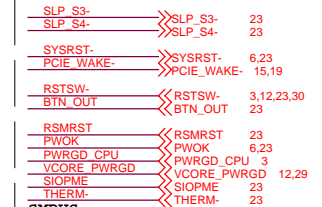
SBB



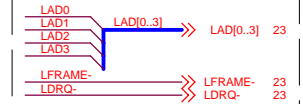
SBD



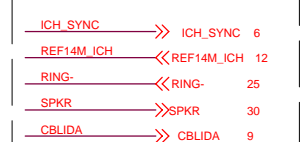
ACPI



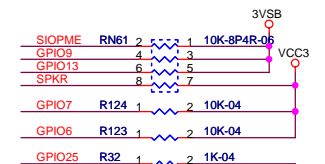
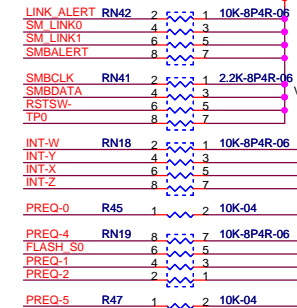
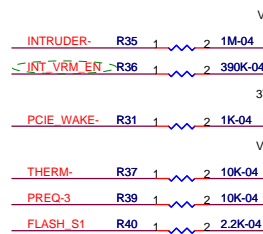
LPC



Others



Strap to Enable
Internal SUS VRM



FLASH_S1	FLASH_S0	Flash Cycle
0	1	SPI
1	0	PCI
1	1	LPC

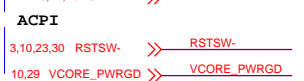
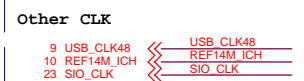
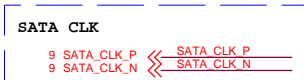
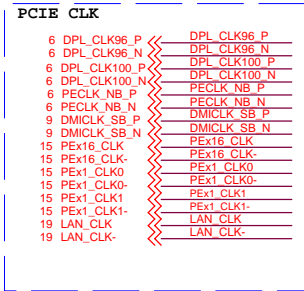
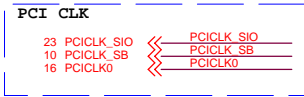
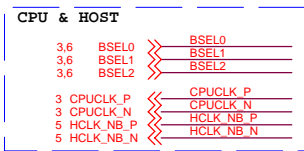
	H	Floating	DESCRIPTION
AZ_SDOUT	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select
AZ_SYNC	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select

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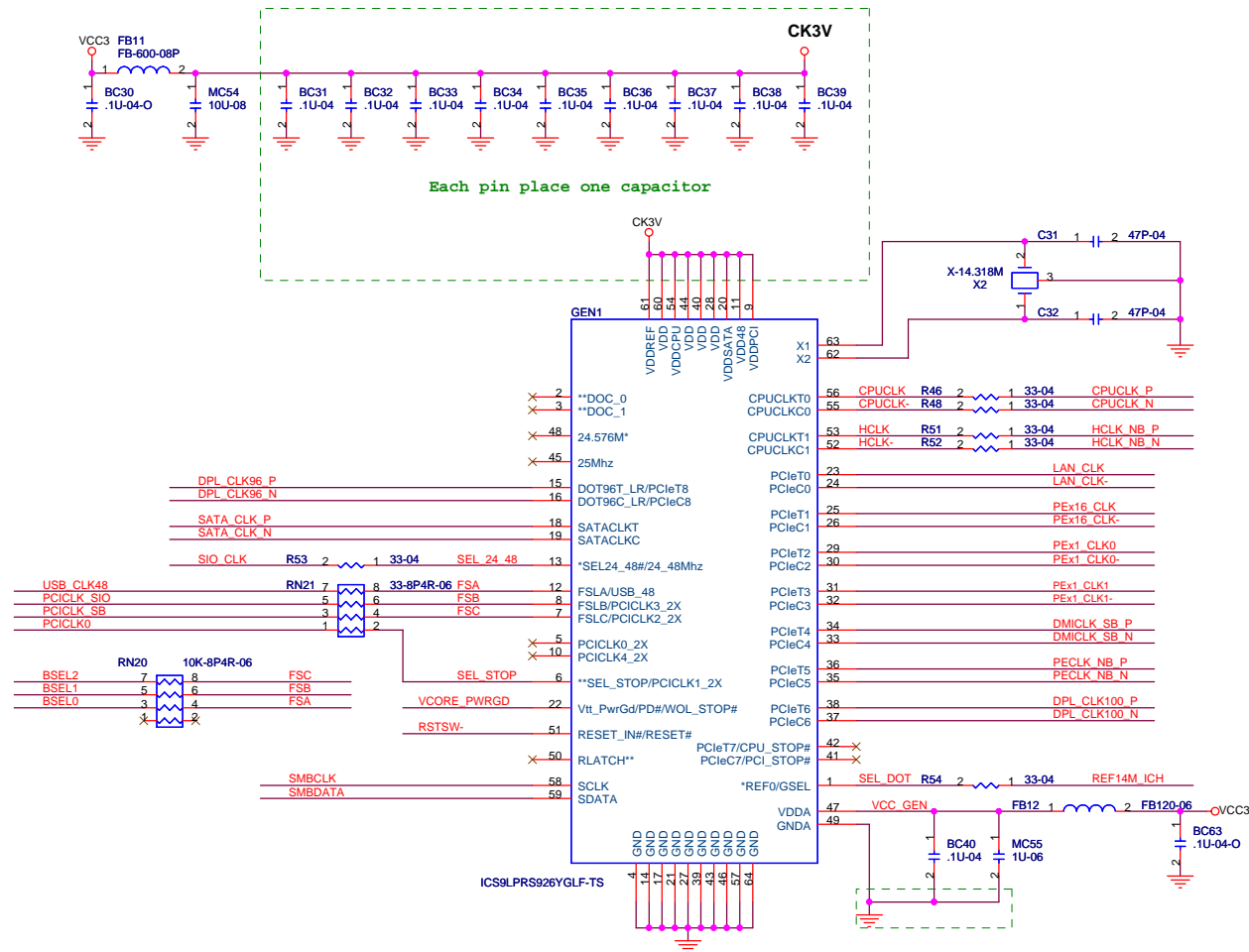
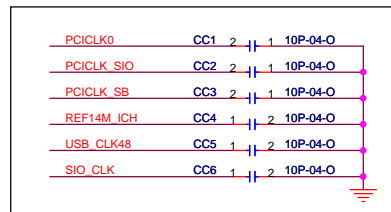
Size: Custom Document Number: **G41T-M** Rev: **7.1**

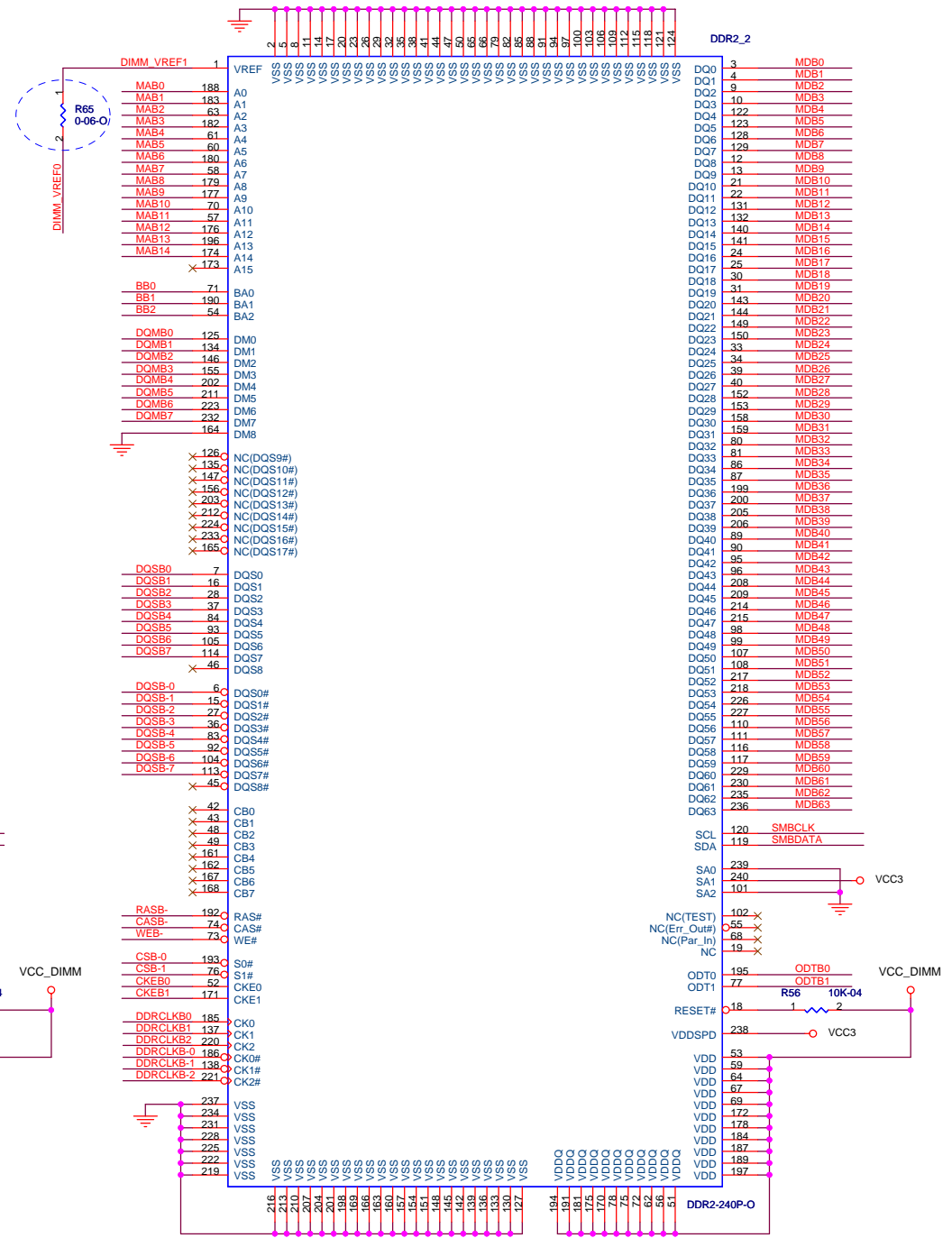
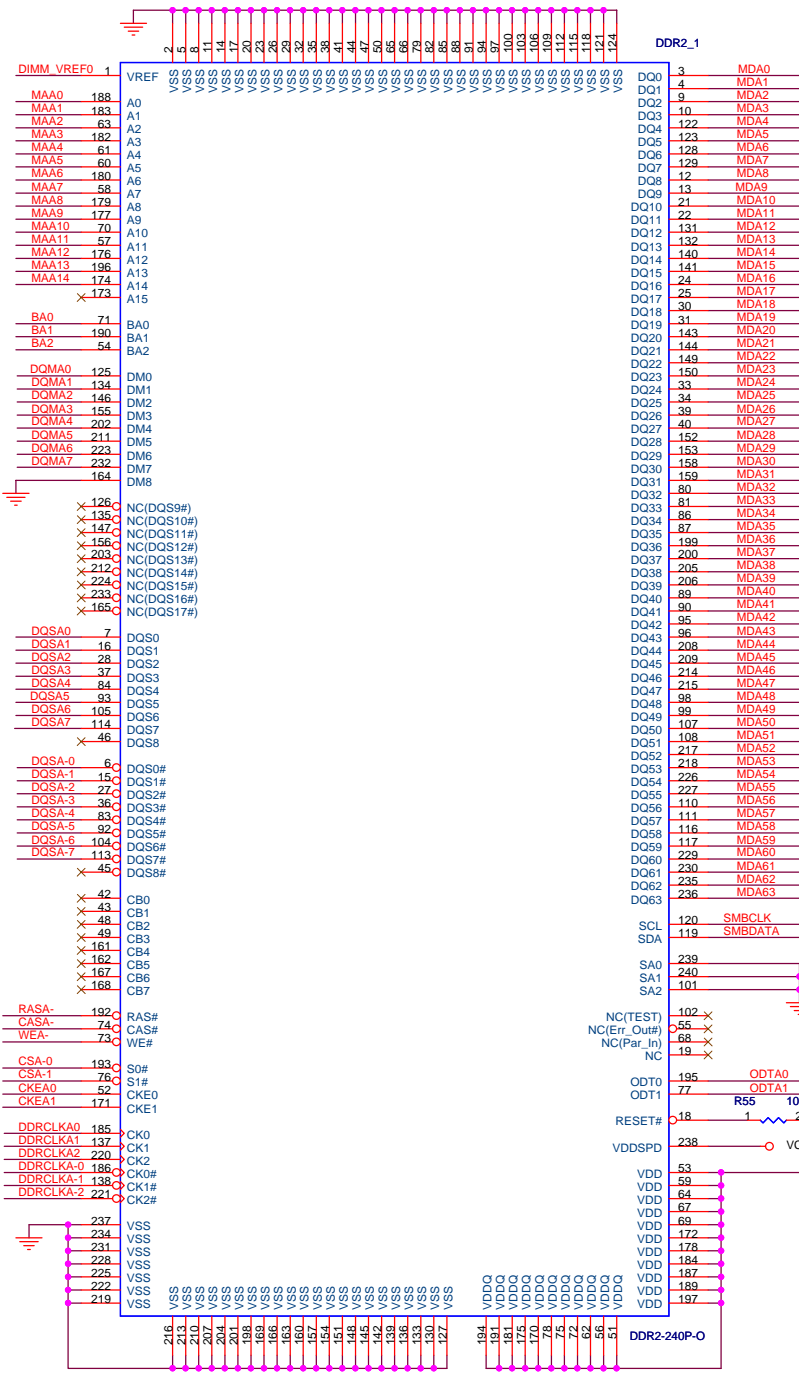
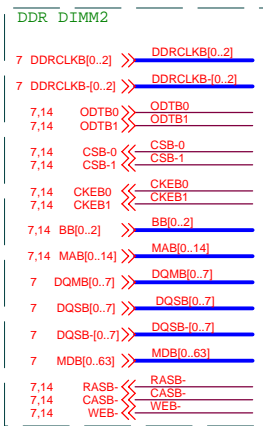
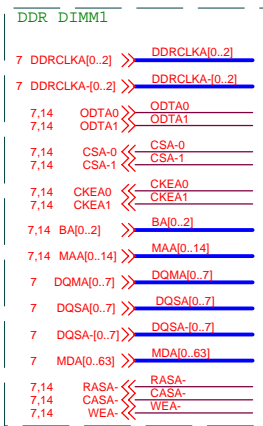
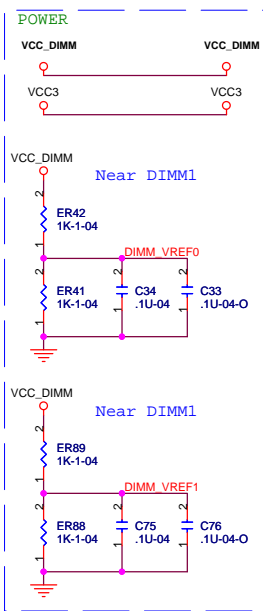
Date: Monday, October 12, 2009 Sheet 10 of 30

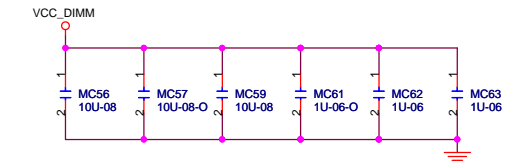
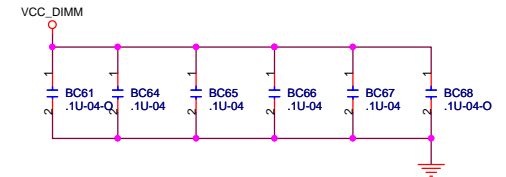
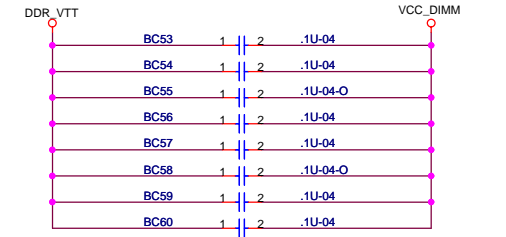
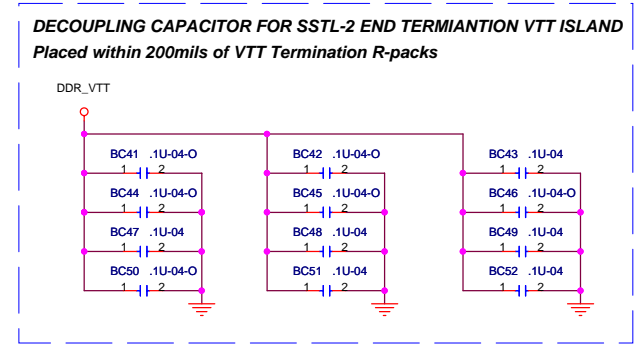
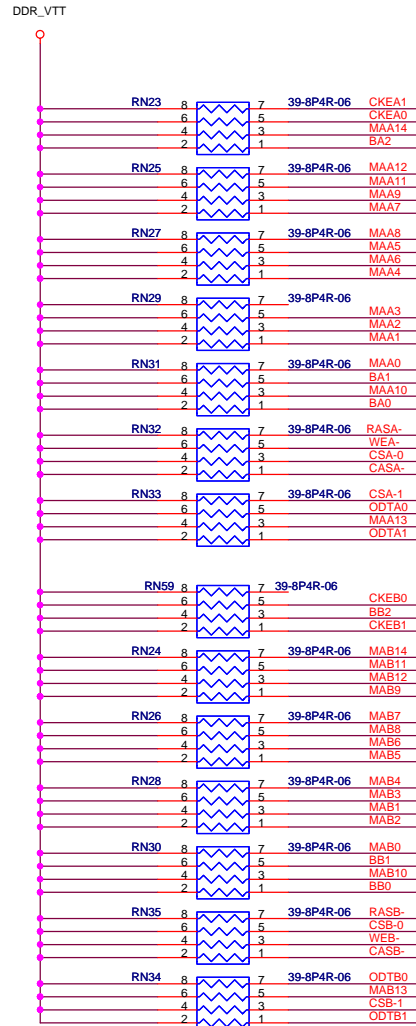
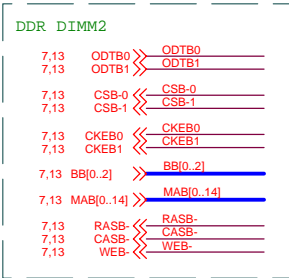
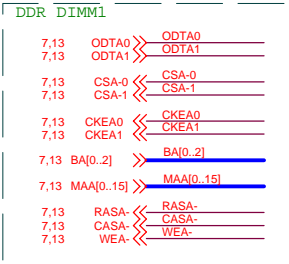


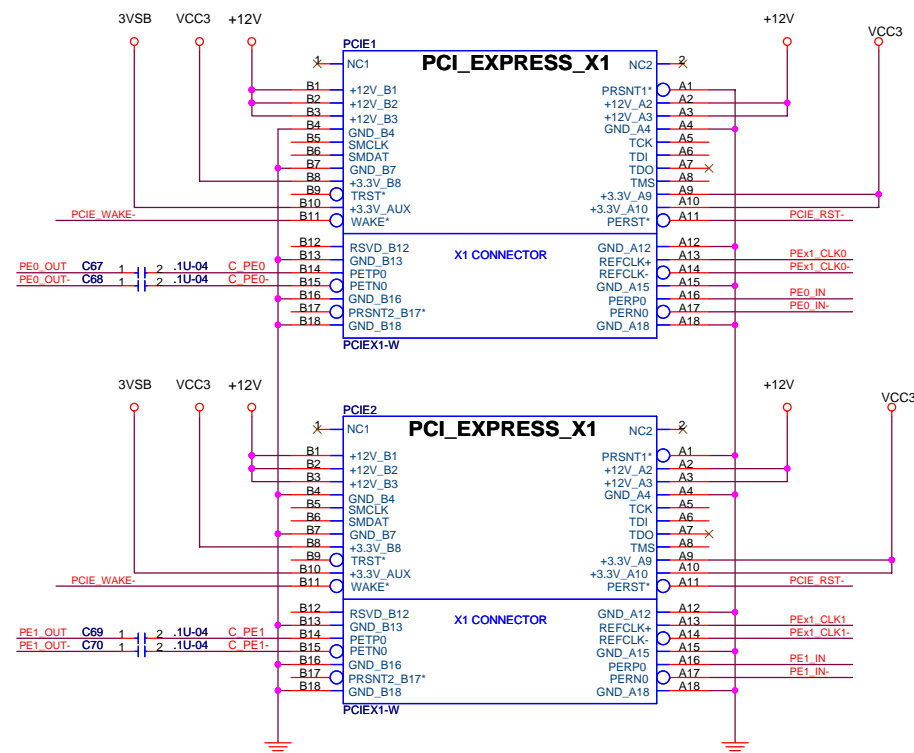
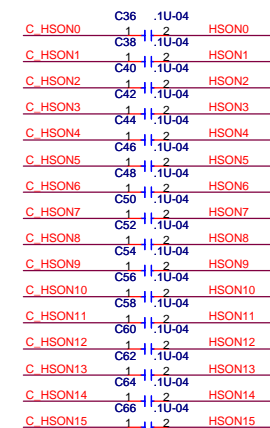
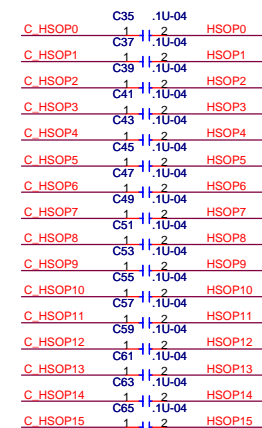
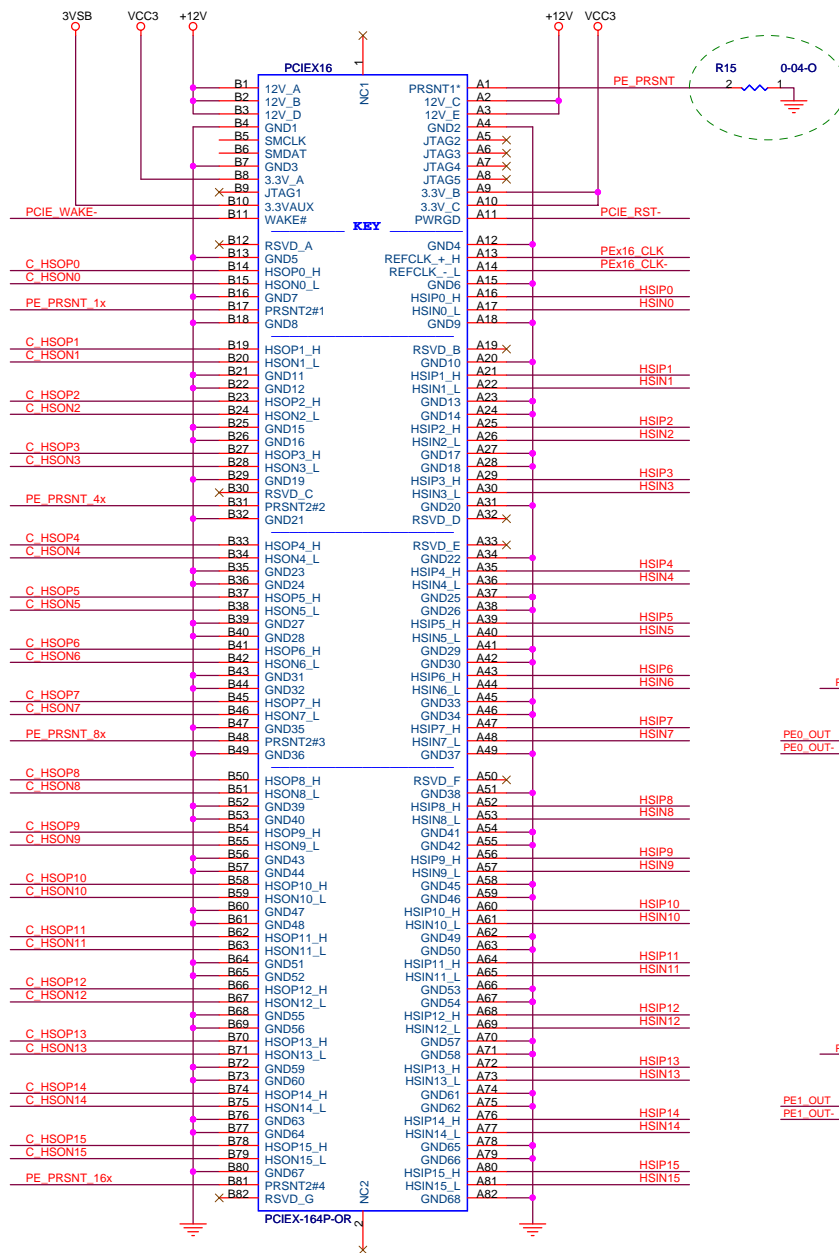
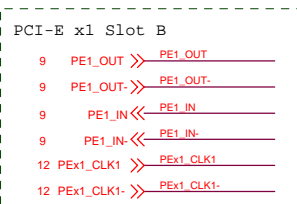
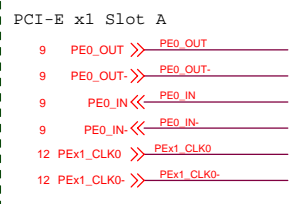
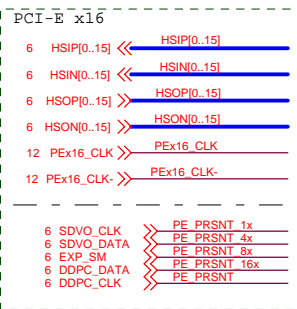
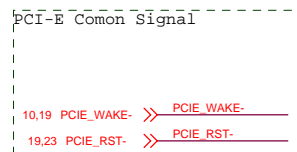
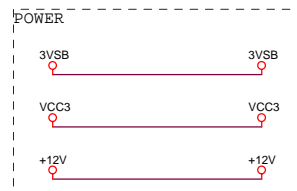
BSEL TABLE			
BIT2 FSLC	BIT1 FSLB	BUT0 FSLA	FSB (CPU) FREQ.
0	0	0	266 MHZ (1066)
0	1	0	133 MHZ (800)
1	0	0	333 MHZ (1333)

HW Strapping		
	0	1
SEL_32K_24M	X	24.576M
SEL_STOP	Pin41,42: PCIE CLK	Pin41,42: STOP Fun
SEL_DOT	DOT=100M	DOT=96M
SEL_24_48	48M	24M

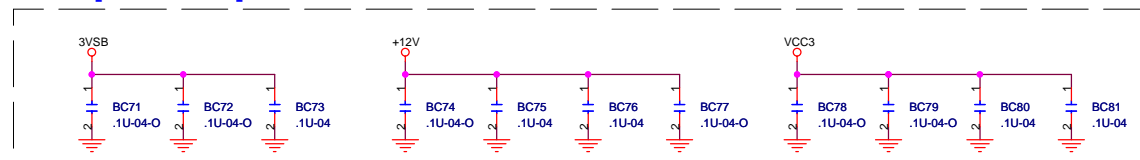




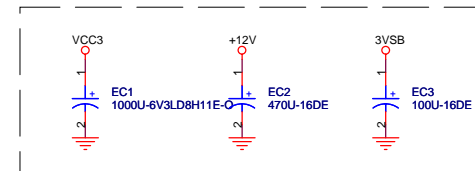


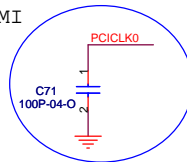
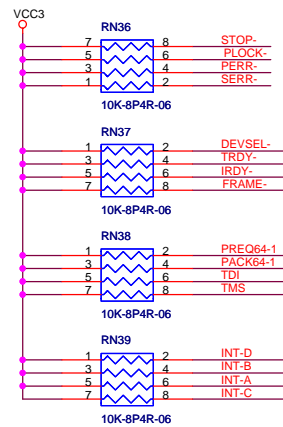
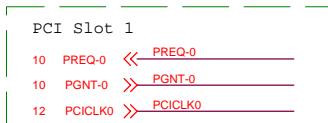


Please place the caps close to PCI-E Slot.

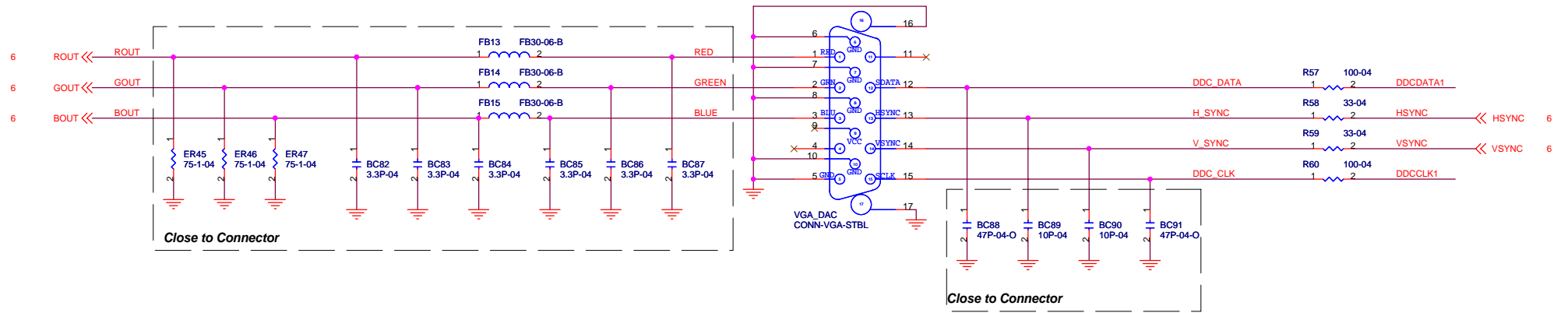


Please place the caps close to PCI-E Slot.

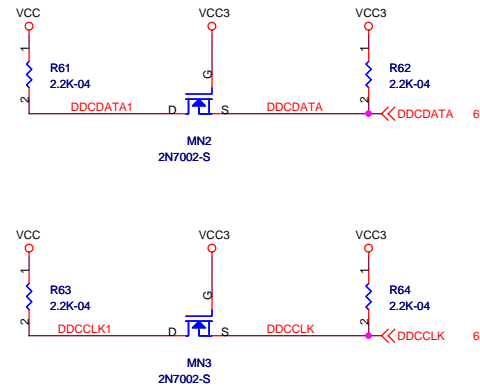




Schematic diagram of capacitor C74, a 0.1uF capacitor connected between 3VSB and ground.

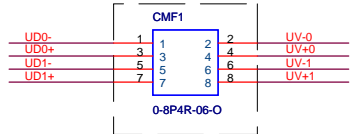
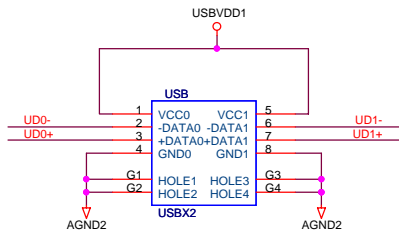
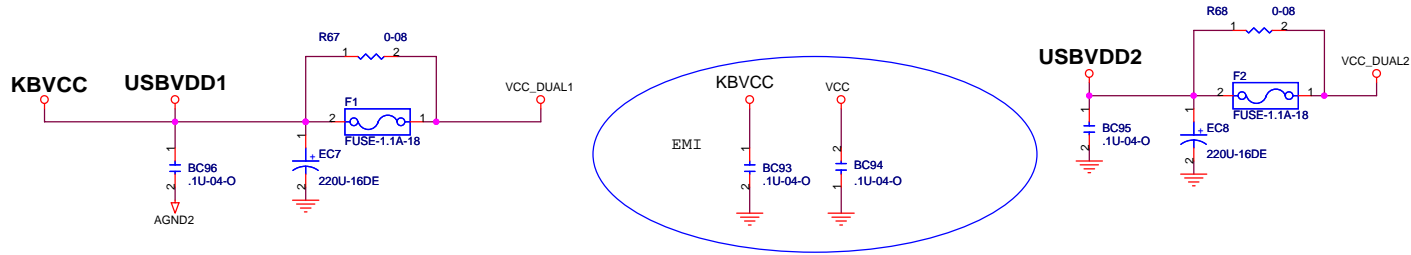
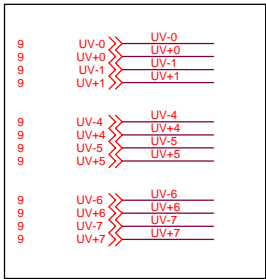


They Can Put Near Connector or Chipset Side, By Placement State

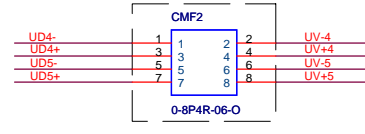
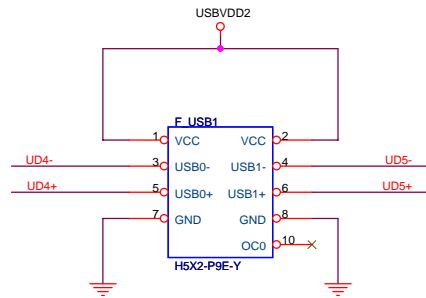


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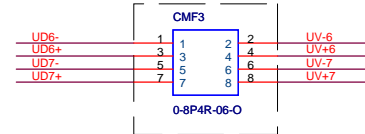
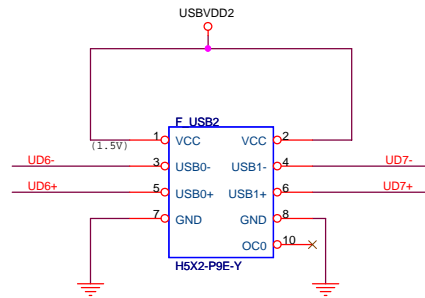
Title		17-VGA (RGB & HDMI)	
Size	Document Number	G41T-M	
Date:	Monday, October 12, 2009	Sheet	17 of 30
Rev	7.1		



Close to USB connector



Close to header(F_USB1)

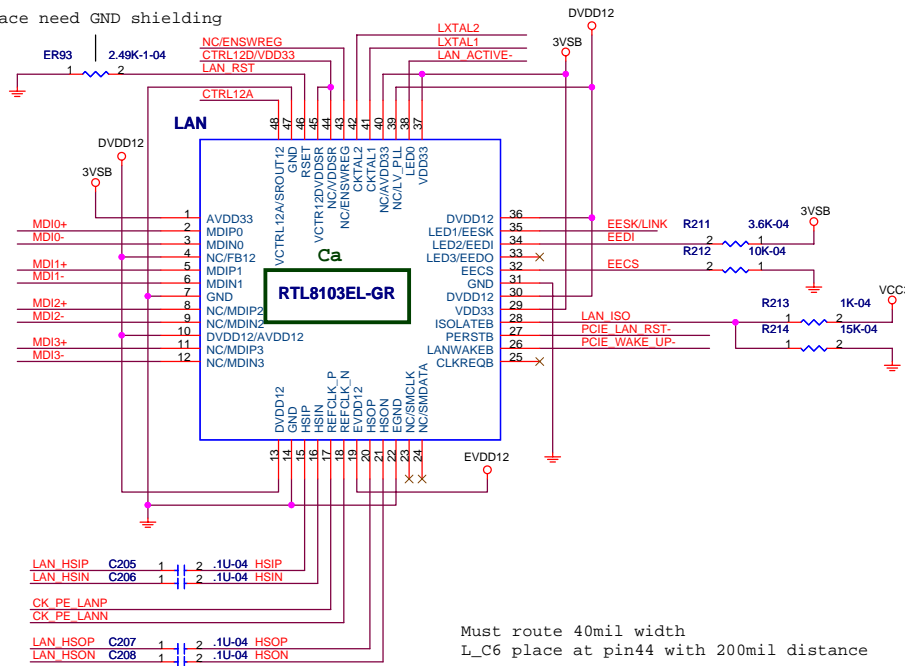


Close to header(F_USB2)

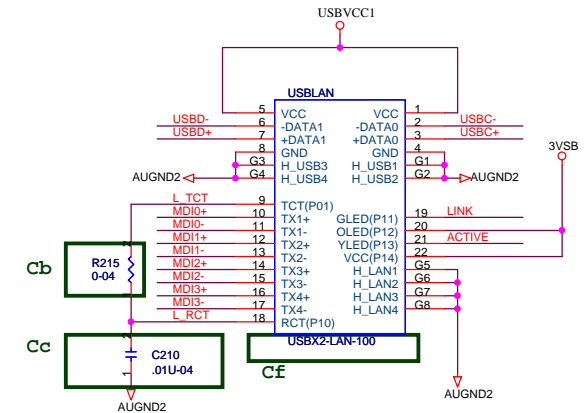
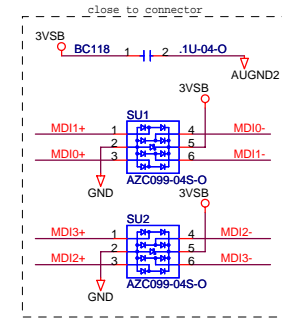
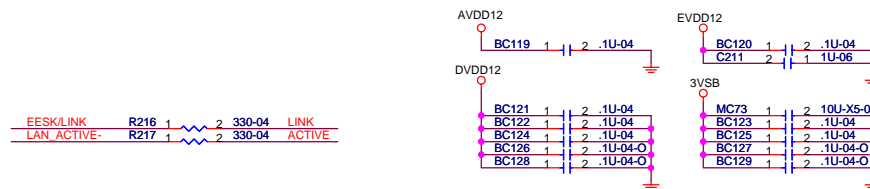
Pinout diagram for USB Type-C connector:

- USBVDD1 to USBVCC1
- 3VSB to 3VSB
- VCC3 to VCC3
- AGND2 to AUGND2
- 10,15 PCIE_WAKE_15,15 to PCIE_WAKE_UP
- 15,23 PCIE_RST_15,23 to PCIE_LAN_RST
- 9 PE3_OUT to LAN_HSP
- 9 PE3_OUT to LAN_HSN
- 12 LAN_CLK to CK PE LANP
- 12 LAN_CLK to CK PE LANN
- 9 PE3_IN to LAN_HSOP
- 9 PE3_IN to LAN_HSON
- 9 UV+2 to USB C+
- 9 UV-2 to USB C-
- 9 UV+3 to USB D+
- 9 UV-3 to USB D-

RSET電阻需close to LAN
Trace need GND shielding



CTRL12D/VDD33 C209 1 2 .1U-04



Pin connection diagram for the 0-8P4R-06-O connector:

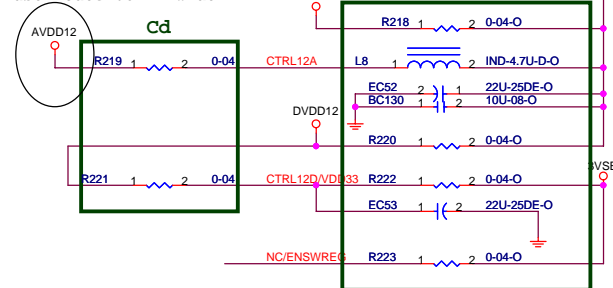
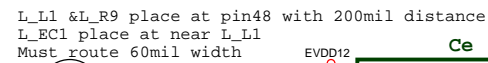
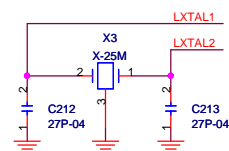
USB Pin	Connector Pin	USB-C Pin
USB C+	8	USBC+
USB C-	6	USBC-
USB D+	4	USB D+
USB D-	2	USB D-

Connector Label: CMF4
Connector Part Number: 0-8P4R-06-O



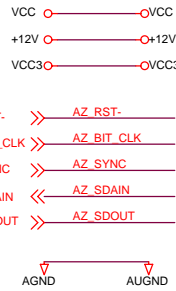
	RTL8111DL-GR 1000M	RTL8103EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8103EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

	RTL8111D	RTL8103E
AVDD33 VDD33	3.3V 3V3B供應	3.3V 3V3B供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

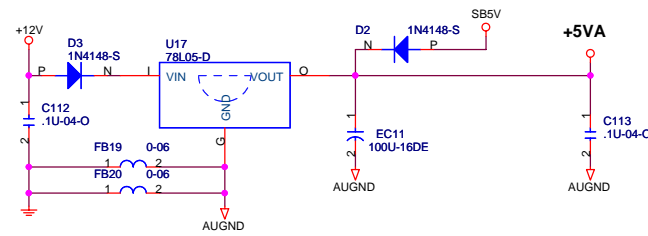


Choke near pin48,
E/C cap near Choke

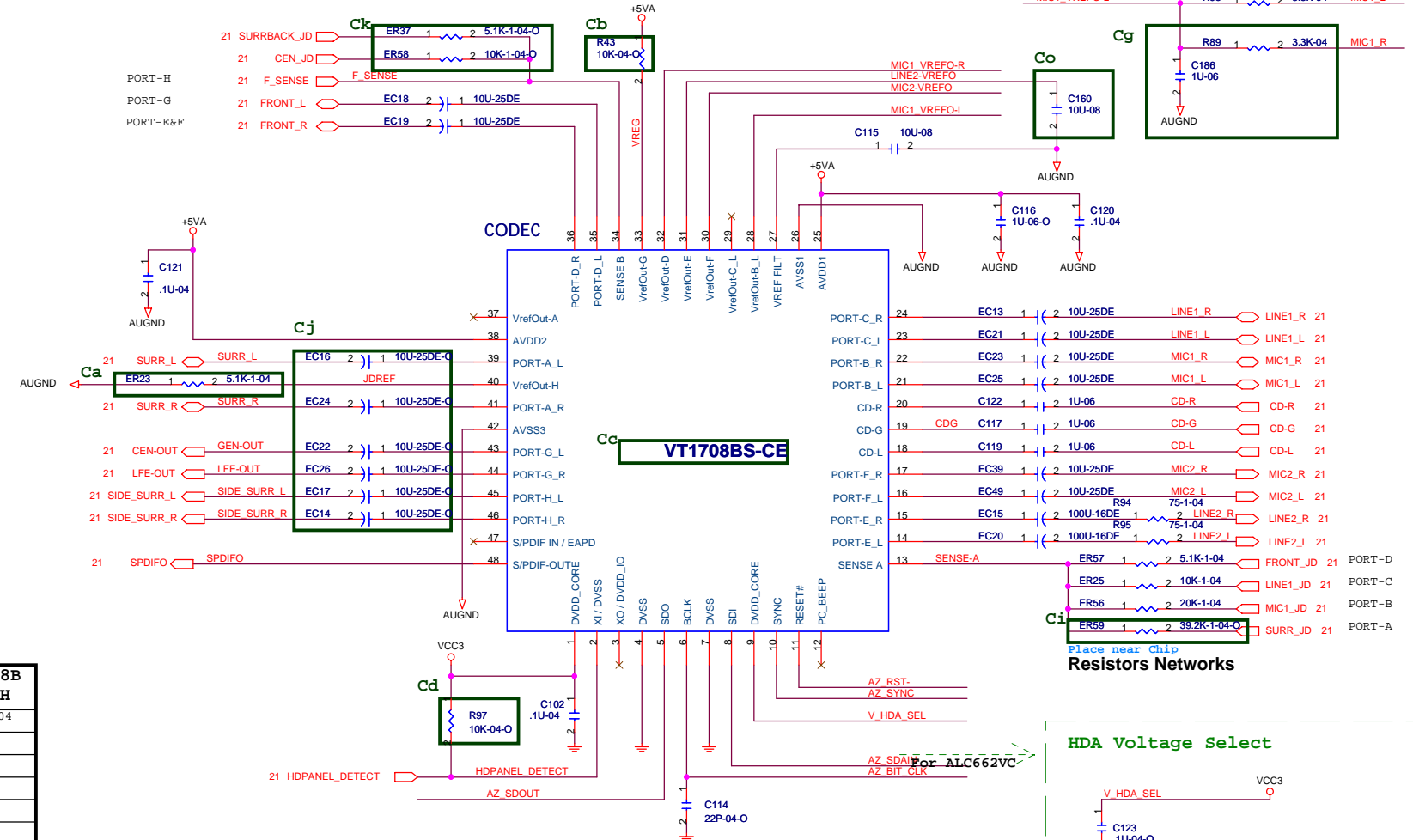
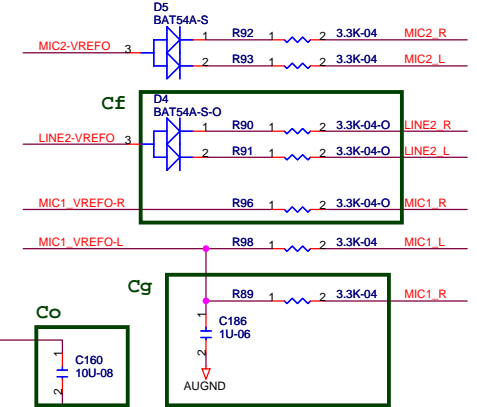
External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.



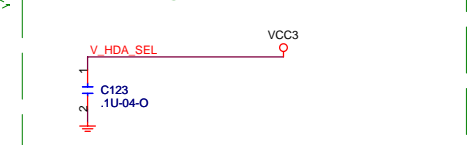
MIC Bias



BOM Difference

Location	ALC662VC 5.1 CH	VT1708B 5.1 CH	VT1708B 7.1 CH
Ca	20K-1-04	5.1K-1-04	5.1K-1-04
Cb	V	X	X
Cc	ALC662-VC-GRS	VT1708BS	VT1708BS
Cd	V	X	X
Cf	V	X	X
Cg	X	V	V
Ch	X	X	X
Ci	X	X	V 7.1CH
Cj	X	X	V
Ck	X	X	V
Cl	X	X	V
Cm	AUDIO-3P-HDA	AUDIO-3P-HDA	AUDIO-6P
Co	X	V	V

HDA Voltage Select



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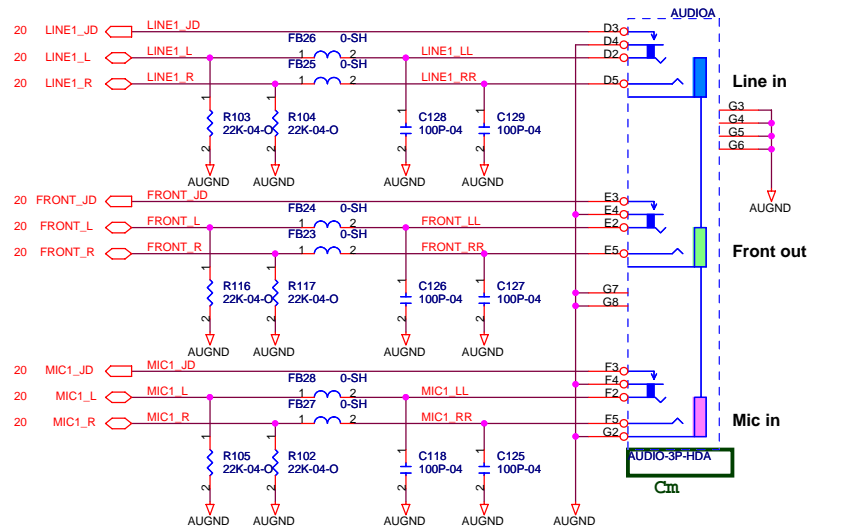
20-Audio Codec (VT1708B)

File	Document Number	Rev
Size	Custom	7.1

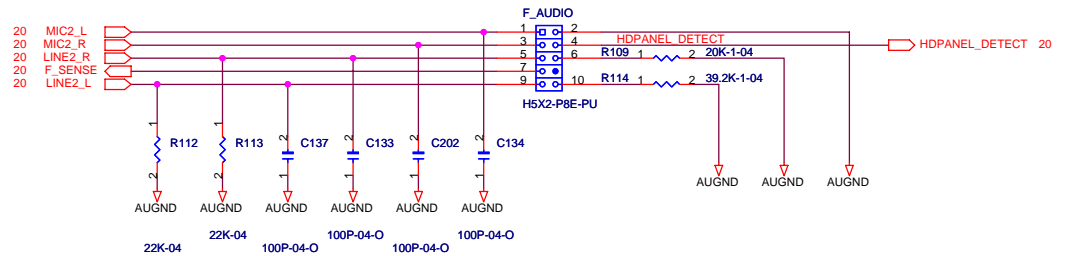
G41T-M

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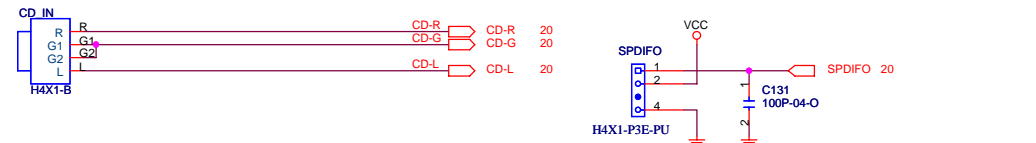
REAR-AUDIO



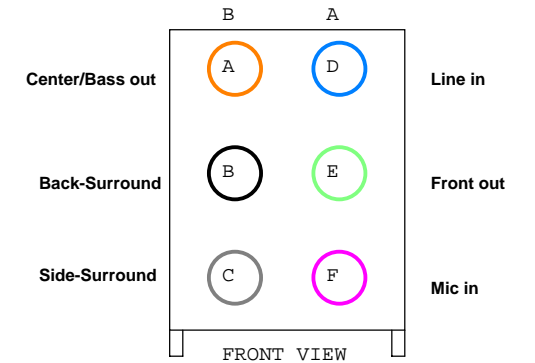
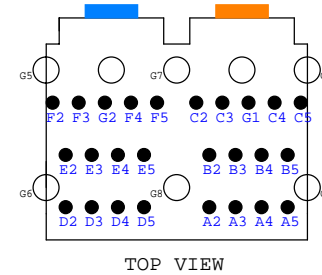
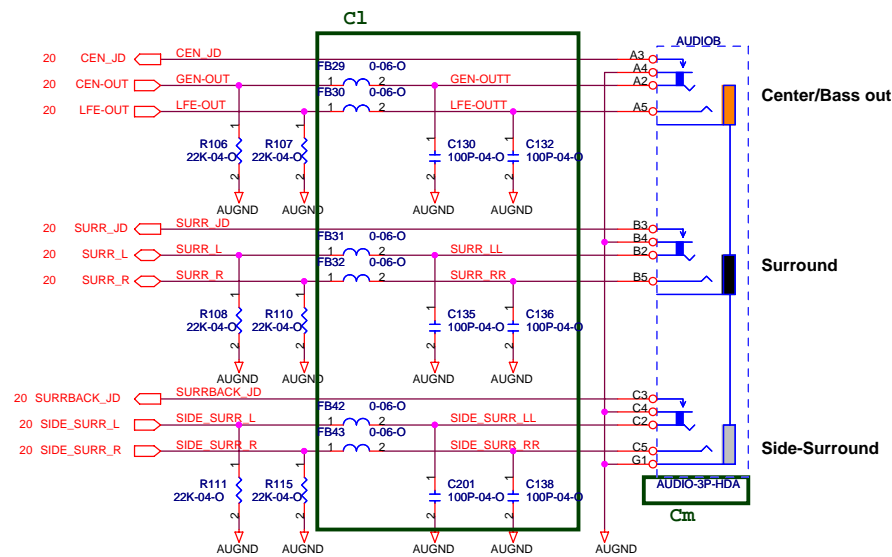
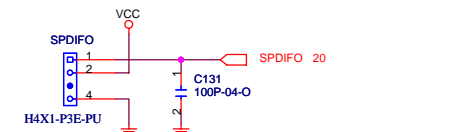
FRONT-AUDIO



CD_IN



SPDIF-OUT



PCB Impedance control			
Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg
60	5 (20/5/20)	6	2116
50	4 (50/4/50)	6	1080
42	6 (50/6/50)	6	1080

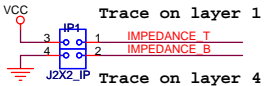
1)Circuit type 1

Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM



For 104

SPI_ROM_D(104)

SPI-ROM-D-8M

BT(104)

+KTS
LITHIUM BATTERY
CD2032
CR2032

CLR_CMOS(1-2)

JP-R

USBPWR_R(1-2)

JP-Y

USBPWR_F(1-2)

JP-Y

NB(104)

HS-38X36X25-SL

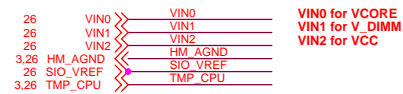
If need 25mm hight :
20-120-010937 or 20-120-011420

For 103

X1(wire)

JP-WI-P6.25

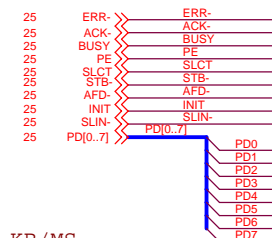
HW Monitor



COM



LPT

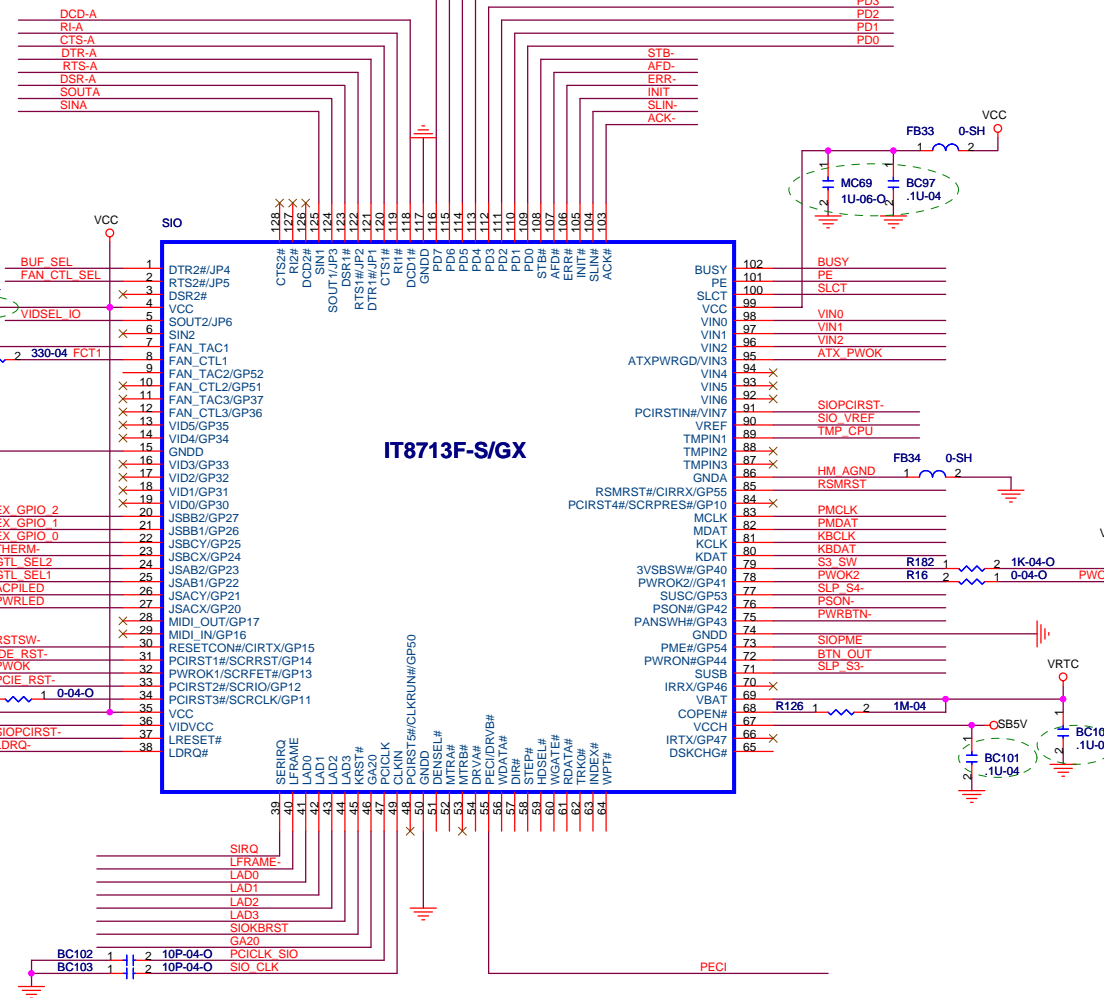


KB / MS

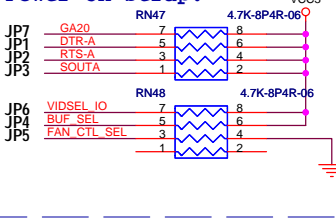


IT8713Power On Strapping Options

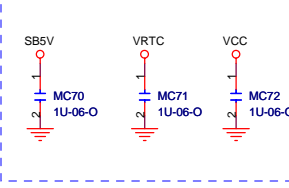
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3	CHIP_SEL		Chip selection in Configuration
JP4	BUF_SEL	1	Output Buffer of PCIRST are open-drain
		0	Output Buffer of PCIRST are push-pull
JP5 : JP7	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 00h
		10	The default value of EC Index 15h/16h/17h is 40h
		01	The default value of EC Index 15h/16h/17h is 20h
		00	The default value of EC Index 15h/16h/17h is 7Fh
JP6	VID_SEL	1	Threshold V of VID is 2.0/0.8 V
		0	Threshold V of VID is 0.8/0.4 V
JP7	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK



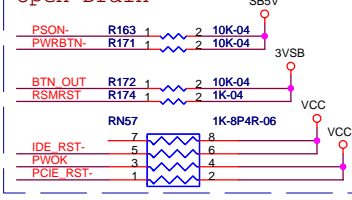
Power On Strap.



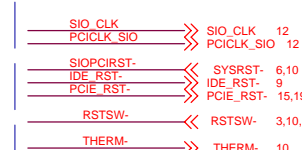
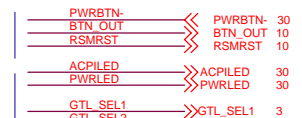
Place Near To SIO Power Pin



Open Drain



ACPI & Others



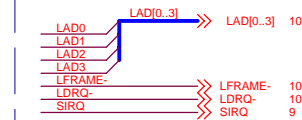
PECI



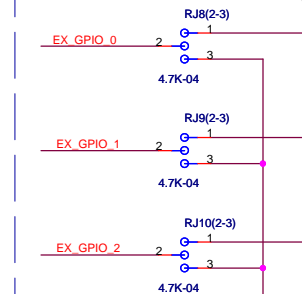
SMART FAN



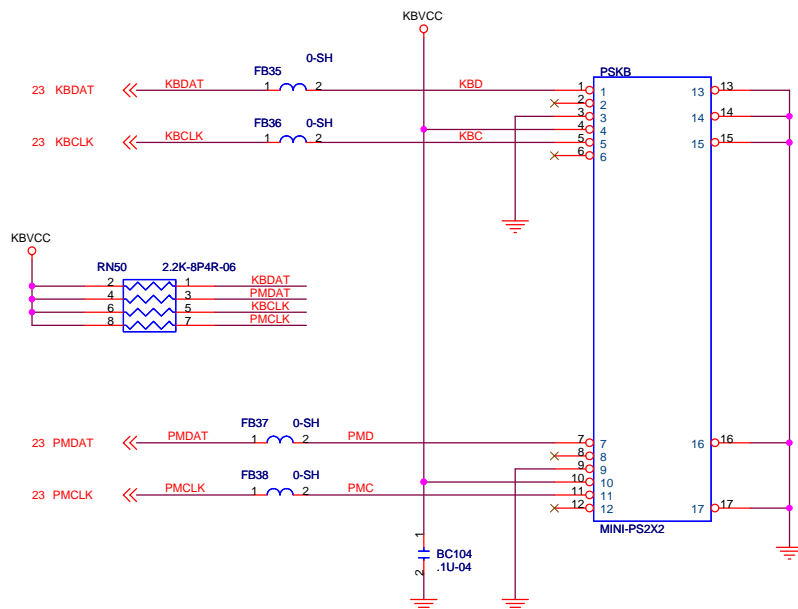
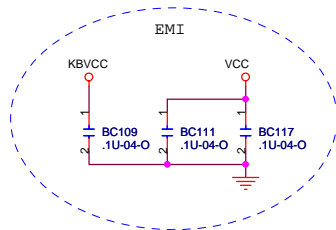
LPC



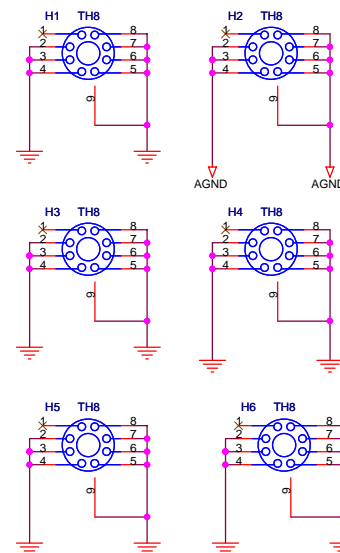
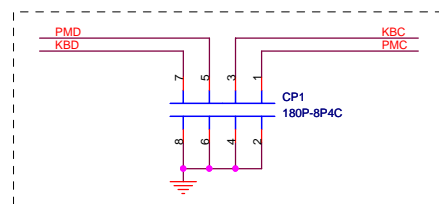
GPIO

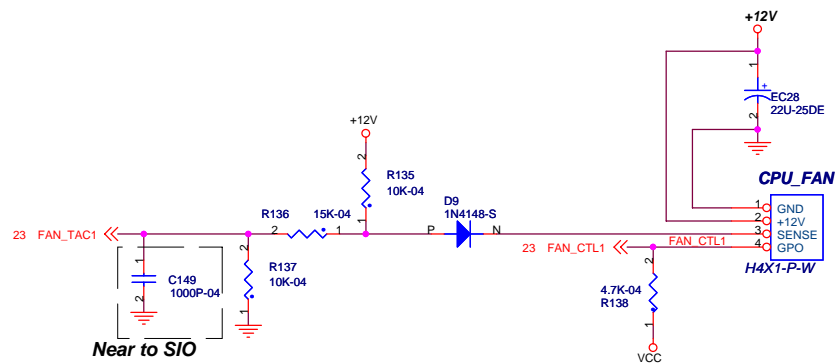


EX_GPIO_0 =0 -> LPT HW Enable
EX_GPIO_0 =1 -> LPT HW Disable

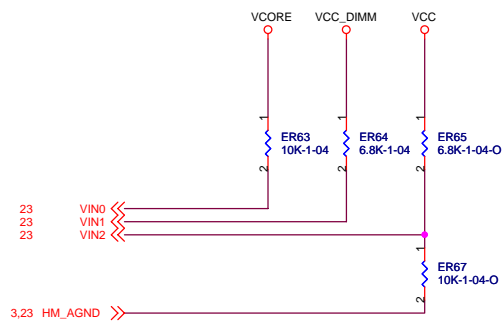


PLACE NEAR CONNECTOR



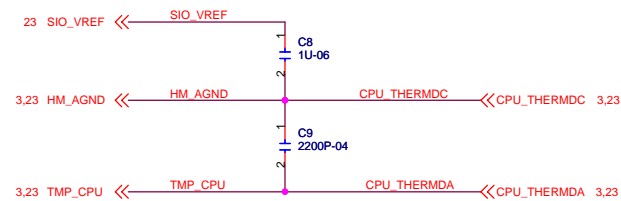


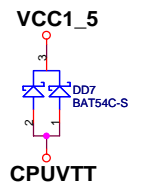
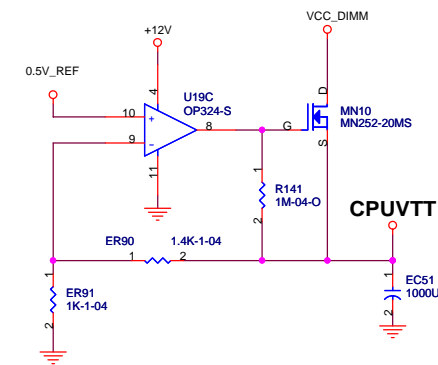
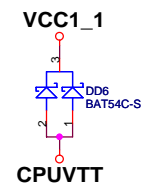
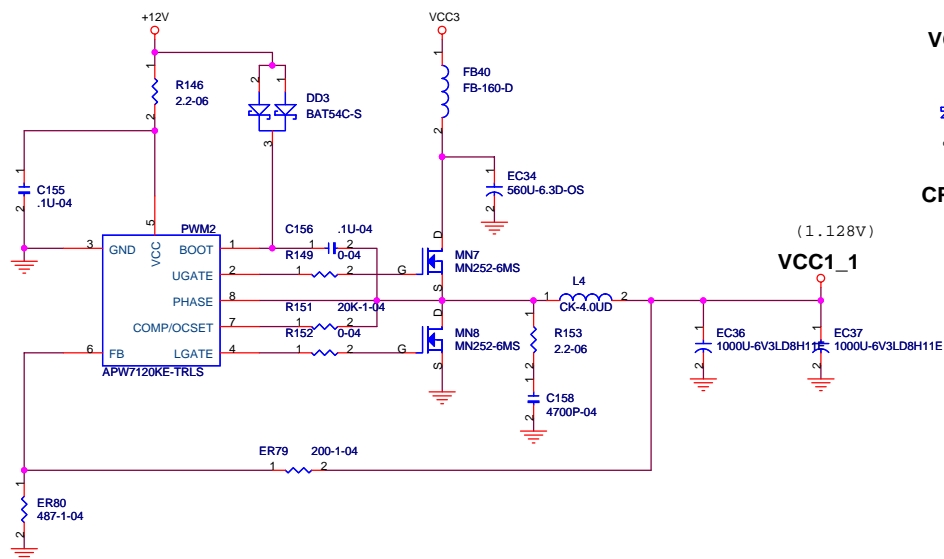
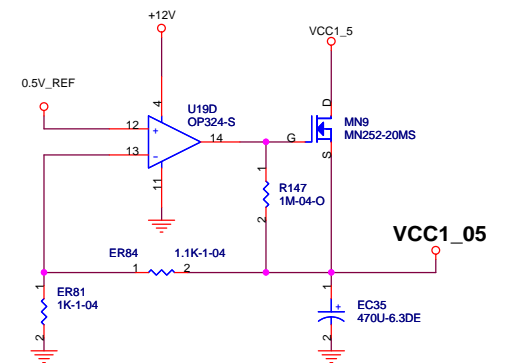
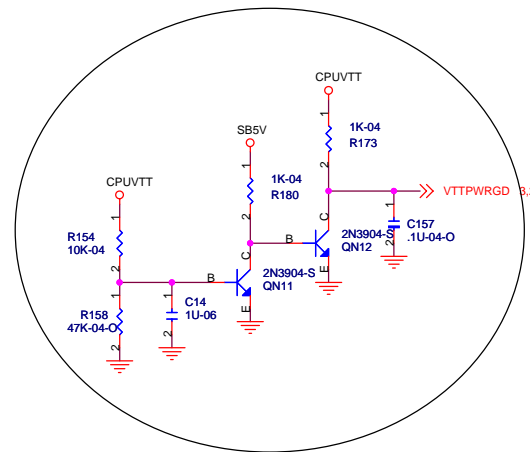
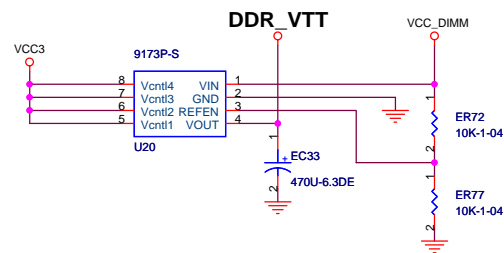
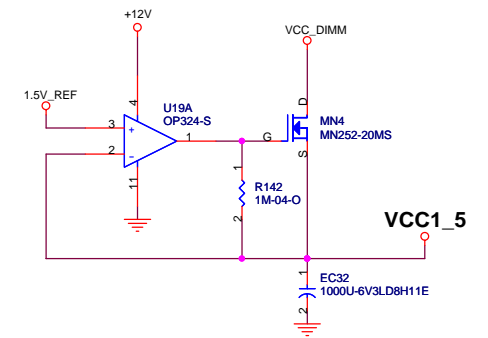
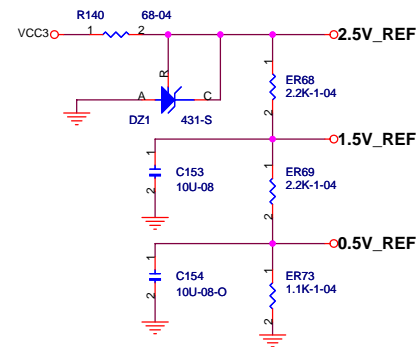
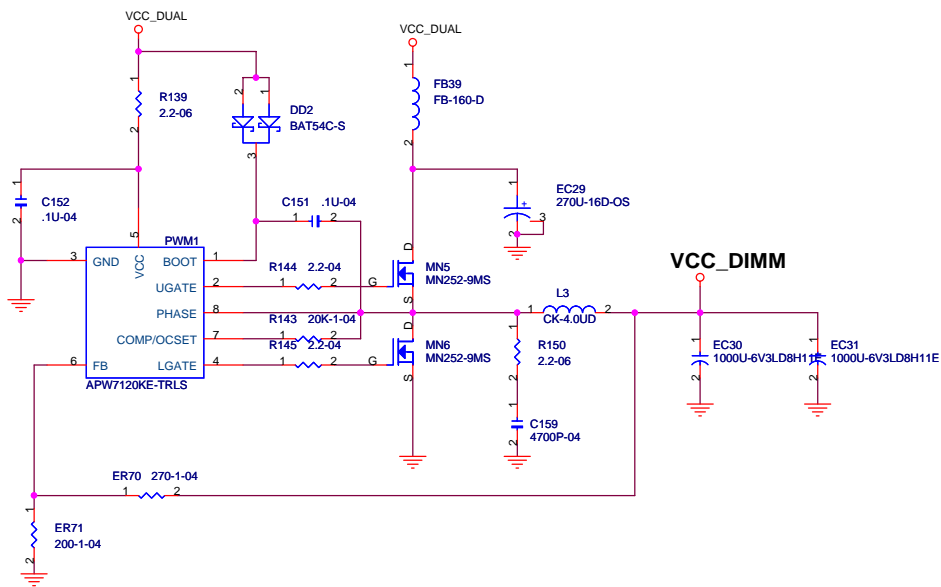
Voltage Monitor

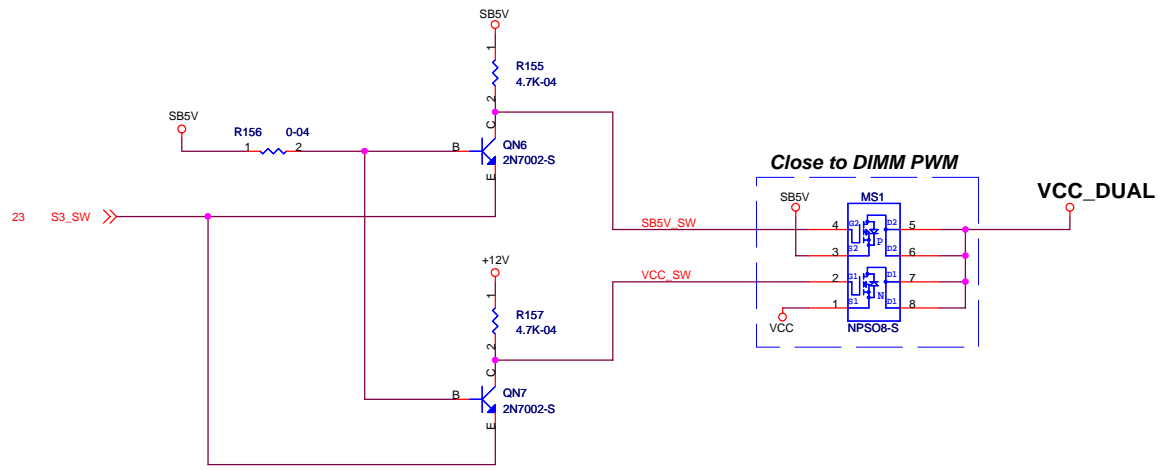
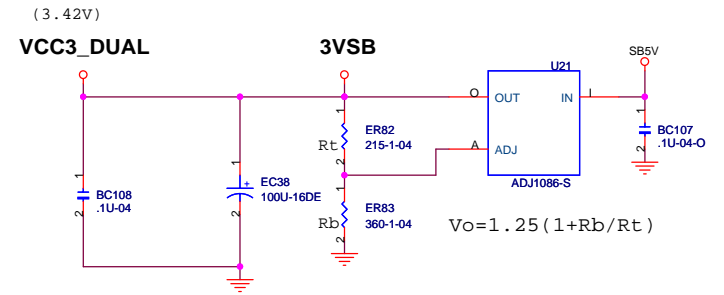
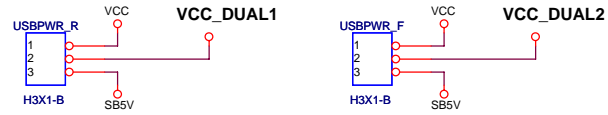


Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode







Memory Power Output Control

	VCC_DUAL	ATX_PWOK	SLP_S4-	SLP_S3-	S3_SW
S0	VCC	1	1	1	1
S1	VCC	1	1	1	1
S3	SB5V	0	1	0	0
S4	0	0	0	0	1
S5	0	0	0	0	1

